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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new non-provisional applications under 37 CFR 1.53(b))

Attorney Docket No. 42390.P6202 Total Pages 2

First Named Inventor or Application Identifier Sanjay Dabral

Express Mail Label No. EL388636058US

ADDRESS TO:	**Assistant Commissioner for Patents** **Box Patent Application** **Washington, D. C. 20231**

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 11)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 7)

4. ___ Oath or Declaration (Total Pages ___)
   a. ___ Newly Executed (Original or Copy)
   b. ___ Copy from a Prior Application (37 CFR 1.63(d))
   (for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**
   i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. _ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. _ Microfiche Computer Program (Appendix)

7. _ Nucleotide and/or Amino Acid Sequence Submission

(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ____ Assignment Papers (cover sheet & documents(s))
9. ____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
   ____ b. Power of Attorney
10. ____ English Translation Document (if applicable)
11. ____ a. Information Disclosure Statement (IDS)/PTO-1449
    ____ b. Copies of IDS Citations
12. ____ Preliminary Amendment
13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. ____ a. Small Entity Statement(s)
    ____ b. Statement filed in prior application, Status still proper and desired
15. ____ Certified Copy of Priority Document(s) (if foreign priority is claimed)
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17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

____ Continuation ____ Divisional ____ Continuation-in-part (CIP)

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18. **Correspondence Address**

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Application for United States Patent

for

An Inline and "Y" Input-Output Bus Topology

by

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"Express Mail" mailing label number: EL388636058US

Date of Deposit: December 29, 1999

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Field

The present invention is directed to circuit boards, and more particularly, bus topologies for circuit boards.

Background

With increasing processor clock rates in the personal computer, workstation, and server industry, there is a pressing need to provide high speed, economical bus topologies. In particular, designing for high speed and economical communication among more than one processor or agent connected to a bus presents various challenges.

Over the years, many bus topologies have been designed. For example, Fig. 1 illustrates a "3D" topology (e.g., vertical cards on a motherboard give the interconnect a 3D nature) in which processor modules **102**, along with their associated heat sinks **104**, are mounted on processor cards **106**, which are connected together to chip set **108** via bus **109** on motherboard **110**. (In an actual embodiment, bus **109** and other traces indicated in Fig. 1 may not be visible.) The connections between an agent, such as a microprocessor, and a bus are often referred to as stubs, and are indicated by numeral **112** in Fig. 1. For some applications, the stub lengths for the 3D topology of Fig. 1 are too long, resulting in undesirable signal reflections.

Yet another bus topology is illustrated in Fig. 2, sometimes called a "2.5D" topology (because there is less vertical dimension when compared to the 3D topology of Fig. 1). For this topology, components (processors or agents) **202**, along with their associated heat sinks **204**, are mounted on both sides of motherboard **206**, facing each other, using connectors **210**, and are connected to chip set **208** via bus **209**. A stub is identified by numeral **212**, but not all stubs are shown. Such topologies are relatively expensive due to motherboard assembly costs. Also, for the topology of Fig. 2, some of the stubs may be too close to each other, so that signal reflections pose a more serious problem.

Busses with many traces may also present design challenges. Some prior art bus topologies use many layers in the motherboard to route the bus traces to chip packages. However, this adds to motherboard complexity and cost. Alternatively, some prior art bus topologies route the bus traces on only one layer or a few layers of the motherboard. But because the dimension of the chip package is often smaller than the physical width

occupied by the bus traces when deposited on one layer, some of the stubs may be too long for some applications.

Embodiments of the present invention are directed to addressing these problems.

Brief Description of the Drawings

Fig. 1 illustrates a prior art bus topology.

Fig. 2 illustrates another prior art bus topology.

Fig. 3 provides an edge view of an embodiment of the present invention.

Figs. 4a and b provide two plan views illustrating an embodiment of the present invention having an inline topology.

Figs. 5a and b provide edge and top views, respectively, of an embodiment of the present invention having a "Y" topology.

Fig. 6 provides a plan view of a bus trace positioned above a conductive plane with de-gassing holes according to an embodiment of the present invention.

Fig. 7 provides a plan view of another embodiment of the present invention.

Detailed Description of Embodiments

Fig. 3 provides an edge view of an embodiment of the present invention. Mounted on one side of motherboard (substrate) **302** are agents **304**, such as, for example, microprocessors. These agents communicate via bus **306** and stubs **308** with chip set **310**. For simplicity, only one trace for bus **306** is shown, and only one stub is shown for each agent. In practice, bus **306** will comprise several or more traces, and each agent may be connected to bus **306** via many stubs. (Bus **306** may not be visible from an edge view of an actual embodiment.) In the particular embodiment of Fig. 3, agents **304** are mounted on connectors **310** and are substantially colinear in their placement upon the motherboard. Agents **304** are mounted with their faces substantially parallel to the face of motherboard **302**. In this way, stubs **308** are kept relatively small in length.

Figs. 4a and 4b provide additional views of the embodiment of Fig. 3. Fig. 4a provides a top pictorial view of agent **406** comprising die **402** and package **404**, where the arrow indicates the general bus direction with respect to the orientation of die **402** and package **404**. As seen from Fig. 4a, the direction of the bus lines is substantially parallel to the edge of package **404**. Also, die I/O pads **418** should be near the periphery of die

402 so that they are close to package pins **420** so as to shorten stub lengths and to allow an easier escape pattern.

Fig. 4b provides a plan view of vias **408** for agent **406** with respect to a direction perpendicular to motherboard **302**. For simplicity, agent **406** is not shown in Fig. 4b, and only three stubs are explicitly shown. In practice, many or all of vias **408** may be connected to stubs. In the example of Fig. 4b, four bus traces or lines **410**, **412**, **414**, and **416** are routed with respect to the via orientation as shown. In Fig. 4b, bus traces **410**, **412**, **414**, and **416**, and vias **408**, may not necessarily lie in the same plane.

In general, for the embodiment of Fig. 4b and other embodiments, vias **408** define a regular array. The region between two consecutive rows (or columns) of a regular array of vias define a channel. For the embodiment of Fig. 4b and other embodiments, bus lines are routed so as to be within or underneath one and only one channel. That is, in an area or region of a board directly underneath a agent that is to be connected to a bus, individual bus traces making up the bus do not cross from one channel to the next. For the particular embodiment shown in Fig. 4b, bus traces **410** and **412** are in one channel, and bus traces **414** and **416** are in another channel. Bus topologies such as those according to the embodiments of Figs. 3, 4a, and 4b allow for relatively small stub lengths, and are found to address some or all of the problems cited in the Background.

For some applications, the length of the bus lines may introduce relatively large latencies. In such cases, for some embodiments, source synchronous communication may be employed, where the source (bus driver) sends both data and clock signals. In some embodiments, a quad pumped bus protocol may be used, where the ratio of the source synchronous clock rate to a common clock rate is equal to four, for example.

An embodiment for wide busses is illustrated in Figs. 5a and 5b. Fig. 5a provides an edge view of a motherboard **512** having interconnector **514** mounted on it. Chip package **516** is mounted on interconnector **514**. Interconnector **514** provides a connection between chip package **516** and bus traces (not shown in Fig. 5a) on motherboard **512**, where the bus traces occupy a wider width than the dimension of chip package **516**. A plan view from the top of chip package **516** is shown in Fig. 5b, where for simplicity only one bus trace **518** is shown. (Parts of bus trace **518** may not be visible in an actual embodiment.)

In Fig. 5b, bus trace **518** connects with interconnector **514** by way of vias **502** and **504**. Bus trace **518** also extends on interconnector **514**, shown in Fig. 5b, as portions **506** and **508**. This extension of bus trace **518** on interconnector **514** connects with chip package **516** by way of via **509**, and stub **510** provides the connection to die **520**. In some embodiments, bus trace portions **506** and **508** may be linear, whereas in others they may be curved or non-linear, or any combination thereof. In one embodiment, the composition of interconnector **514** is such that the characteristic impedance of the portions **506** and **508** of bus trace **518** on interconnector **514** is substantially equal to the characteristic impedance of bus trace **518** on motherboard **512** so as to reduce signal reflection.

For the embodiment of Figs. 5a and 5b, the stub lengths are relatively short due to the use of interconnector **514**. This reduces signal degradation due to signal reflection. In the particular embodiment of Figs. 5a and 5b, interconnector **514** is on the same side of motherboard **512** as chip package **516**, so that interconnector **514** may be termed an interposer. However, in other embodiments, interconnector **514** may be on the opposite side of motherboard **512** relative to chip package **516**, so that in these embodiments interconnector **514** may be termed an underposer.

Some busses comprise one or more traces and a conductive plane, so that a trace and the conductive plane comprise a structure for guided electromagnetic wave propagation, i.e., a transmission line. The characteristic impedance of a transmission line may be effected by discontinuities in the conductive plane and surrounding dielectric material.

In particular, de-gassing holes are introduced into a conductive plane to allow for gasses to escape, especially during manufacturing. These de-gassing holes present discontinuities in the conductive plane. Often, these de-gassing holes are aligned with each other to form a substantially regular array of holes, but this is not always necessarily the case. Fig. 6 provides a simplified plan view of bus traces **601** and **602** above conductive plane **604** having de-gassing holes **606**.

In the embodiment of Fig. 6, bus traces **601** and **602** are aligned with respect to de-gassing holes **606** such that their characteristic impedances are substantially equal to each other. This may be accomplished by arranging traces **601** and **602** so that they have similar environments. For example, traces **601** and **602** may be routed so that each trace

passes over the same local average of holes per unit length. This local average may be taken over a quarter-wavelength $\lambda/4$. Preferably, the sizing of de-gassing holes **606** are such that they are substantially smaller than the wavelength λ of the electromagnetic wave to be propagated by traces **601** and **602**. For example, the diameter of the de-gassing holes may be less than $\lambda/10$.

For the embodiment of Fig. 6, it is also preferable that variations in the characteristic impedance along the length of a trace are minimized. One approach is to route a trace so that the local average of holes per unit length passed by the trace is substantially independent of position along the trace.

Fig. 7 illustrates another embodiment in which there are two pin fields, denoted by **720** and **722**, for two agents (not shown). Three traces **702**, **704**, and **706** are routed on a circuit board (not shown) and are connected, respectively, to vias **708**, **710**, and **712** in pin field **720**. In many prior art routing techniques, only two traces per channel are routed because each trace may easily connect with vias defining the channel, and thus the embodiment of Fig. 7 represents an improvement over such prior art routing techniques. Note that vias **708**, **710**, and **712** lie within one row of vias. Traces **702**, **704**, and **706** are also routed to second pin field **722** and connect with vias **714**, **716**, and **718**, which also lie within one row of vias.

The row of vias containing via **724** and the row of vias containing via **712** define a first channel in pin field **720**, and the row of vias containing via **712** and the row of vias containing via **726** define a second channel in pin field **720**. As seen in Fig. 7, the traces enter one channel and exit an adjacent channel so that connections to the vias do not need to overlap the other traces. Routing multiple traces per channel reduces printed circuit board costs.

The embodiment of Fig. 7 may be extended to other embodiments with more than three traces in which vias within one row are to be connected to the traces. Furthermore, the connected vias need not be adjacent to one another. Also, there may be other layers in the circuit board in which other traces are deposited and routed so that traces enter one channel and exit and adjacent channel.

Various modifications may be made to the disclosed embodiments without departing from the scope of the invention as claimed below.

What is claimed is:

1. A circuit board having two sides, the circuit board comprising:

a substrate having a first array of vias to connect to a first agent, the first array of vias defining a first set of channels on the substrate, and having a second array of vias to connect to a second agent, the second array of vias defining a second set of channels on the substrate; and

a bus comprising bus traces, wherein each bus trace is routed in only one channel belonging to the first set of channels and routed in only one channel belonging to the second set of channels.

2. The circuit board as set forth in claim 1, wherein the first and second agents are mounted upon only one of the two sides of the circuit board.

3. The circuit board as set forth in claim 1, wherein the bus propagates a source synchronous clock signal having a source synchronous clock frequency and a common clock signal having a common clock frequency,

wherein the source synchronous clock frequency is at least twice the common clock frequency.

4. The circuit board as set forth in claim 3, wherein the first and second agents are mounted upon only one of the two sides of the circuit board.

5. The circuit board as set forth in claim 1, wherein the first array of vias are arranged in substantially linear rows and the second array of vias are arranged in substantially linear rows.

6. An electronic system comprising:

a circuit board having a first trace segment and a second trace segment; and

an interconnector supported by the circuit board, the interconnector having a third trace segment connected to the first trace segment by way of a first via, and having a fourth trace segment connected to the second trace segment by way of a second via.

7. The electronic system as set forth in claim 6, wherein first, second, third, and fourth trace segments have substantially equivalent characteristic impedances.

8. The electronic system as set forth in claim 6, further comprising:

a die; and

a die package to support the die, the die package having a stub connected to the third and fourth trace segments by way of a third via, wherein the first, second, third, and fourth trace segments form a bus trace.

9. A circuit board comprising:

a conductive plane having de-gassing holes;

a first bus trace substantially parallel to the conductive plane;

a second bus trace substantially parallel to the conductive plane; and

a dielectric disposed between the conductive plane and the first and second bus traces, the combination of the first and second bus traces with the conductive plane and dielectric having, respectively, first and second characteristic impedances and to guide electromagnetic radiation having a wavelength, wherein the de-gassing holes are substantially smaller than the wavelength, and wherein the first and second bus traces are positioned relative to the de-gassing holes so that the first and second characteristic impedances are substantially equal to each other.

10. The circuit board as set forth in claim 9, wherein the de-gassing holes have diameters less than one-tenth of the wavelength.

11. A circuit board comprising:

a conductive plane having de-gassing holes;

a first bus trace substantially parallel to the conductive plane;

a second bus trace substantially parallel to the conductive plane; and

a dielectric disposed between the conductive plane and the first and second bus traces, the combination of the first and second bus traces with the conductive plane and dielectric to guide electromagnetic radiation having a wavelength, wherein the de-gassing holes are substantially smaller than the wavelength, wherein the first bus trace passes over a first local average of de-gassing holes per unit length, wherein the second bus trace passes over a second local average of de-gassing holes per unit length, and wherein the first and second bus traces are positioned relative to the de-gassing holes so that the first

and second local averages of de-gassing holes per unit length are substantially equal to each other.

12. The circuit board as set forth in claim 11, wherein the second and first local averages are taken over one quarter of the wavelength.

13. The circuit board as set forth in claim 11, wherein the de-gassing holes have diameters less than one-tenth of the wavelength.

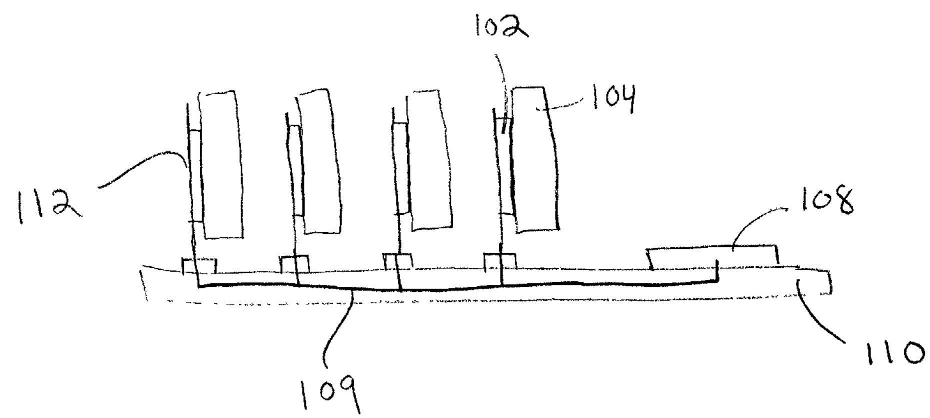
14. A circuit board comprising:

a substrate having an array of vias, the array of vias defining a set of channels on the substrate; and

three bus traces routed on the circuit board so as to enter a first channel belonging to the set of channels and to exit a second channel belonging to the set of channels, the first and second channels adjacent to each other so that there is one row of vias between the first and second channels, wherein each of the three bus traces are connected to a via belonging to the row of vias so as to define three connections, wherein the three connections do not overlap the three bus traces.

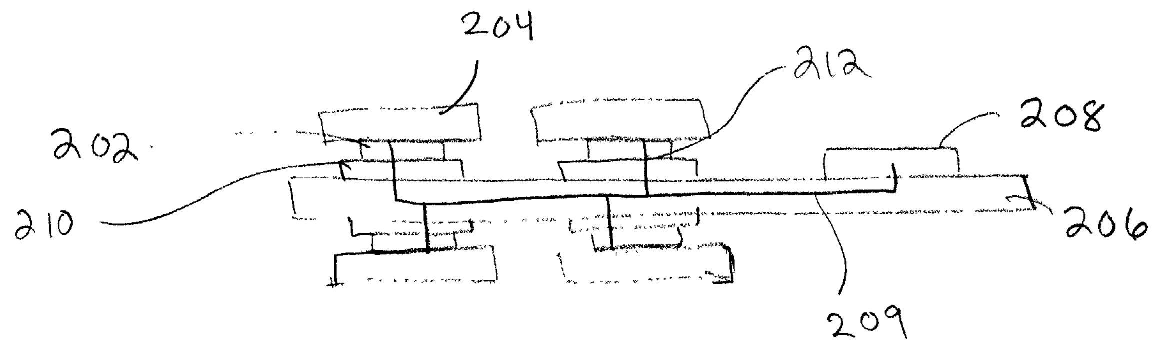
Abstract

Various bus trace topologies are provided which allow for shorter stub lengths, reduced motherboard costs, more efficient routing between multiple agents, and bus traces with better matched characteristic impedances.



(Prior Art)

Fig. 1



(Prior Art)

Fig. 2

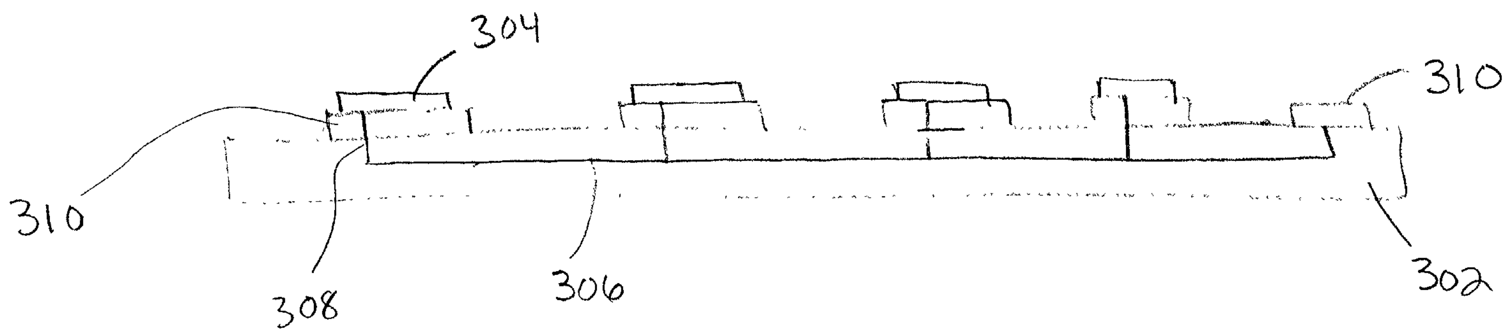
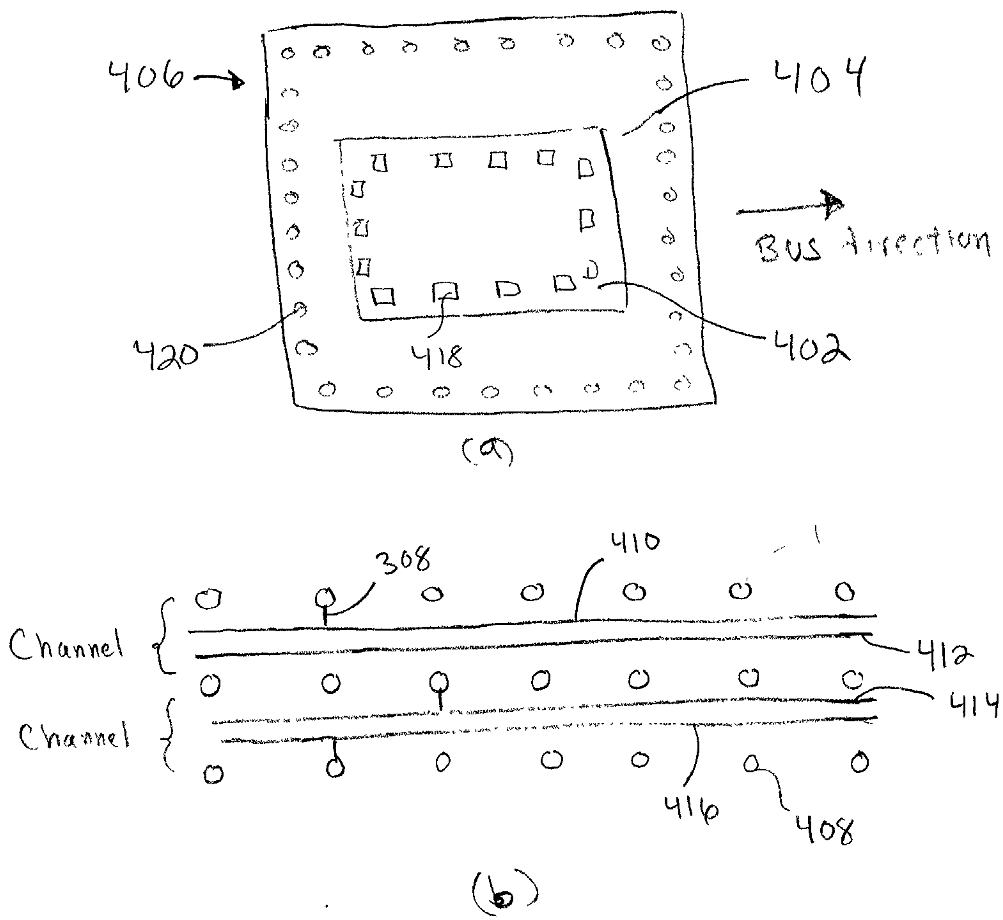


Fig. 3



406
404
Bus direction
420
418
402
(a)
308
410
Channel
Channel
412
414
416
408
(b)

Fig. 4

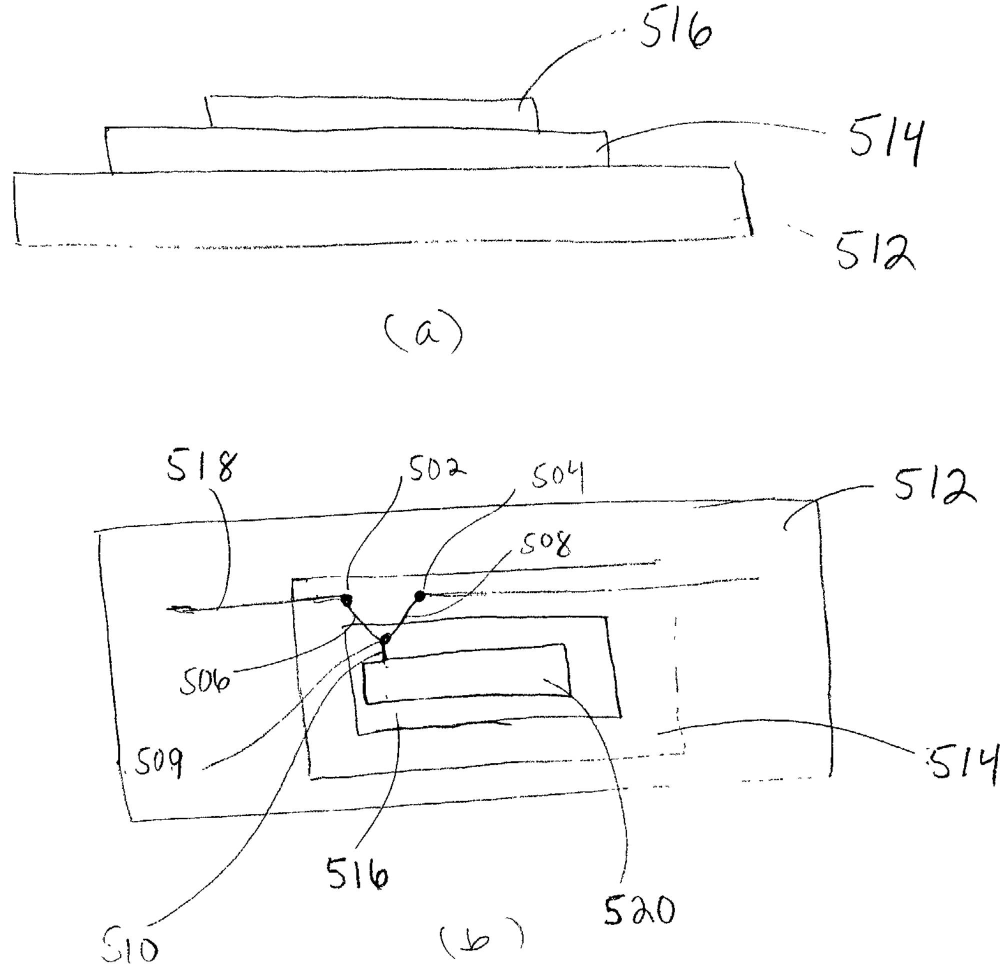


Fig. 5

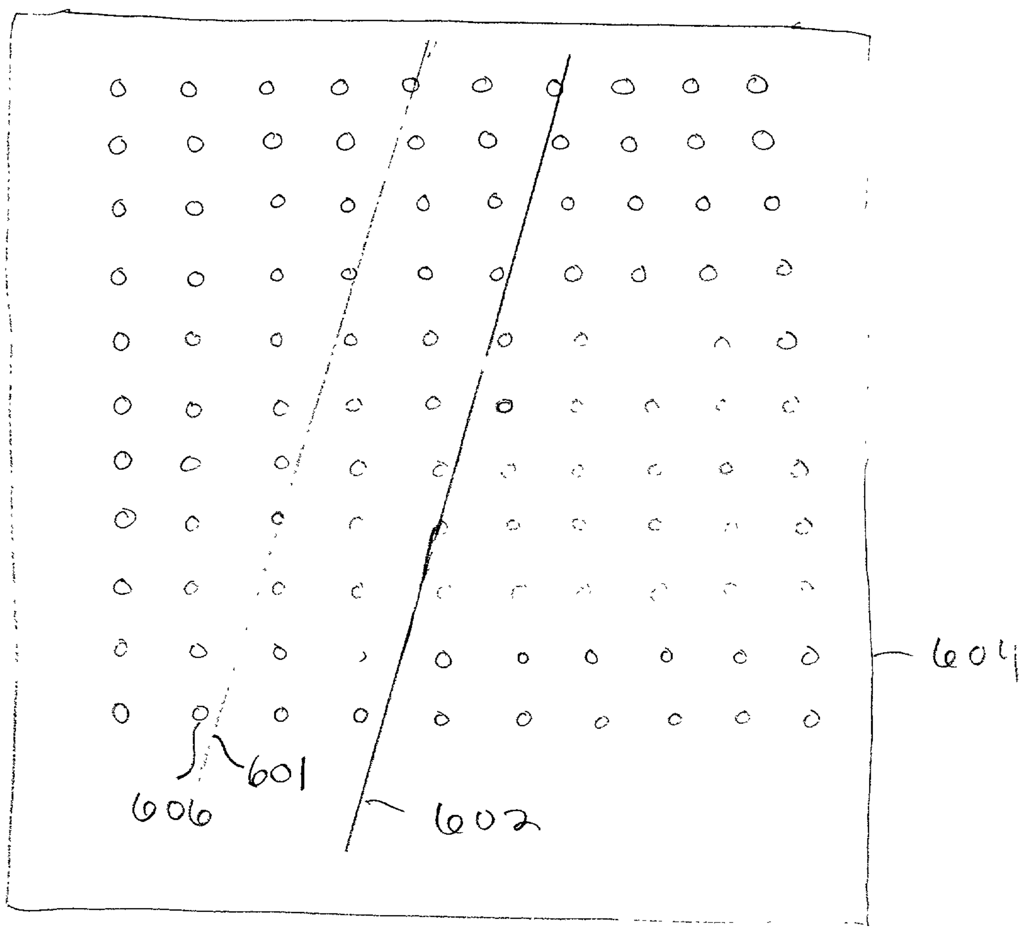


Fig. 6

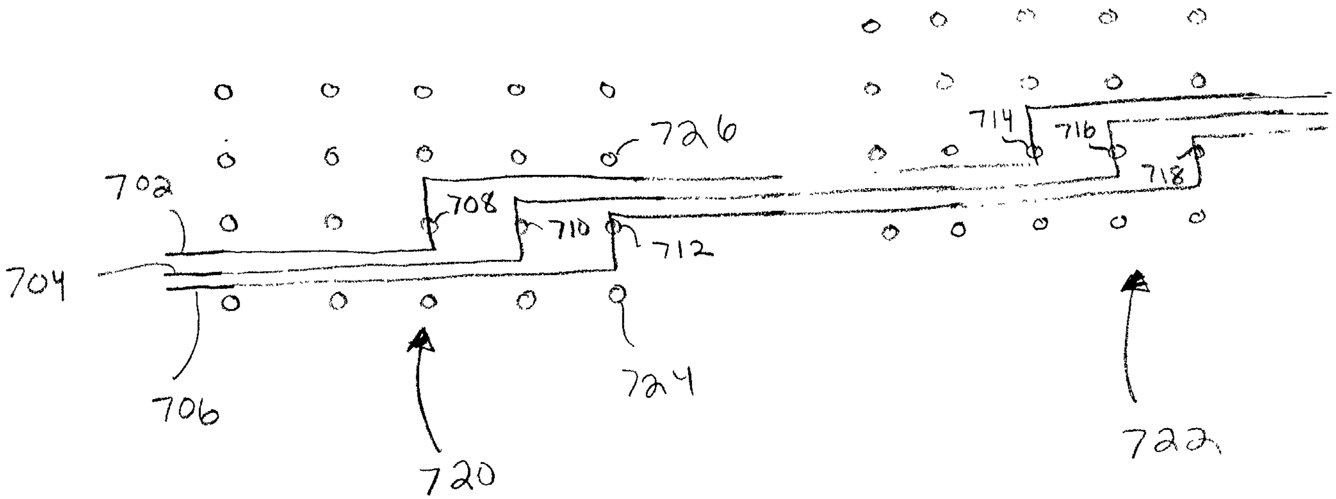


Fig.7